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Design For Test Technique for Leakage Power Reduction in Nanoscale Static Random Access Memory

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Abstract: Problem statement: As technology scales down, the integration density of transistors increases and most of the power is dissipated as leakage. Leakage power reduction is achieved in Static Random Access Memory (SRAM) cells by increasing the source voltage (source biasing) of the SRAM array. Another promising issue in nanoscaled devices is the process parameter variations. Due to these variations, higher source voltage causes the data stored in the cells of the SRAM array to flip (weak cell) in the standby mode resulting in hold failure. The weak cells identified are replaced using redundant columns. Maximum source voltage that can be applied to reduce the leakage power without any failure depends on the number of redundant columns available to repair the weak cells. **Approach:** This study proposes a novel Design For Test (DFT) technique to reduce the number of March tests, thus reducing the test time using a source bias (V_{SB}) predictor. In the proposed method, V_{SB} predictor predicts the initial source bias voltage to be applied to the SRAM array. The proposed DFT verified by designing an 8×16 SRAM array in 90 nm technology. March algorithm was used to identify the weak cells and predict the maximum source voltage from '0' mV. This process was run large number of March tests consuming more test time. **Results and discussion:** The predicted V_{SB} helps to make a fast convergence of maximum V_{SB} to be applied, which will improve the speed performance of the adaptive source bias and saves the test time by 60 %.

Key words: Leakage power, process parameter variations, Design for Test (DFT), nanoscaled devices, SRAM array, architectural level, source voltage, adaptive source biasing, proposed technique

INTRODUCTION

About 70% of the total systems-on-chip (SoCs) area is occupied by the embedded memories (Jayabalan and Povazanec, 2002). Compared to DRAMs, embedded SRAMs are often used in SoC applications due to their higher packaging density (Zorian, 2002). Therefore CMOS SRAMs remains to be the yield limiters in SoCs. When the speed of the devices increases along with the integration density, the leakage power consumption also increases. In addition, as technology scales down, the process parameter variations causes the leakage power consumption to increase exponentially dominating the total power consumption (Pavlov and Sachdev, 2008). Hence, leakage power in the nanometer regime has become a significant portion of power dissipation in CMOS circuits especially in area constrained circuits such as SRAM cell (Salem *et al*., 2010). Leakage power suppression can be done in circuit level and architectural level.

At circuit level, dynamic control of transistor gate-source and substrate-source bias is done to enhance the drive strengths in active mode and low leakage path in stand-by period (Peiravi *et al*., 2009). In these schemes the amount of biasing voltage must be chosen in such a way that it must be lesser than the supply voltage (V_{dd}) if not, it then raises the reliability issues. At the architectural level, constant supply voltage scaling gives the lower energy-delay product but it requires scaling of the threshold voltage (V_{th}) as well, which increases the sub-threshold leakage current, thus increasing the chip's leakage power. The leakage power reduction can be achieved at this level by technique such as gating-off the supply voltage of idle memory sections. The less frequently used memory sections are put into drowsy standby mode and dynamic voltage scaling is applied (Flautner *et al*., 2002). Leakage energy savings of over 70% in the data cache is

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achieved but at the lower bound of standby V_{dd}, the data may be lost. Qin *et al*. (2005), under ultra-low standby $V_{dd,}$ the limit of SRAM data preservation, namely DRV (Data Retention Voltage) is explored. But DRV is a strong function of process parameter variation and may get varied due to technology scaling (Wang *et al*., 2007). Adaptive body biasing is another technique to reduce leakage power in SRAM. Reducing sub-threshold leakage current causes variation in V_{th} resulting in various functional failures in SRAM. These failures can be avoided by adaptively biasing the body since threshold voltage (V_{th}) is a function of body bias (Mukopadhyay *et al*., 2005; Lu and Naing, 2005). However this scheme requires larger bit cell area and overall SRAM area.

Several techniques such as supply voltage scaling, body biasing, source biasing have been proposed to reduce the leakage power in SRAM designs. Among them source biasing is promising because increasing the source-bias voltage (V_{SB}) of source line in SRAM array reduces the leakage power but increases the hold failure (Ghosh *et al*., 2006). The probability of retaining the data at the standby mode decreases mainly due to process parameter variation (in particular, threshold voltage (V_{th})) which happens as technology scales down (Bhavnagarwala *et al*., 2001; Cheng *et al*., 2004). The cells affected due to hold failures are replaced using redundant columns in the SRAM array during testing (Ali and Khamis, 2005). The amount of V_{SB} applied to the source line in SRAM array is very important because V_{SB} in-spite of reducing the leakage power also decide upon the hold failures that would exist in the SRAM array. Hence, V_{SB} is applied based on the number of redundant columns present in the SRAM array. To determine the maximum V_{SB} (maintaining the hold failures under control) and to identify the cells affected due to hold failures, a large number of March tests have to run thus increasing the time complexity of the March algorithm (Ali *et al*., 2005). Hence, in this study an efficient DFT technique with source bias predictor is proposed to reduce the number of March tests while predicting the maximum V_{SB} thus reducing the test time.

This study is organized as follows: following the introduction is the discussion about the impact of source biasing on SRAM with process parameter variations. The proposed DFT technique with V_{SB} predictor and adaptive source biasing is explained further. Finally conclusions are offered and References are noted.

Impact of process parameter variations on SRAM:
In nanoscaled devices, the random variations in the number of dopant atoms in the channel region of the device cause random variations in device parameters. Variations in transistor parameters such as channel length, width, oxide thickness results in die-to-die (inter-die) and within-die (intra-die) variation in threshold voltage of a device. These variations in process parameters can result in threshold voltage mismatch between the transistors on the SRAM array resulting in various failures especially the functional failures such as read, write, access and hold failures. The main reason for hold failure in the SRAM cell is the within-die (intra-die) variation in the threshold voltage (V_t). In addition to functional failures process parameter variations have a strong impact on leakage of the SRAM array (Roy *et al*., 2003).

To analyze the leakage behavior of a SRAM cell, a conventional 6T SRAM cell is designed as shown in Fig. 1.

'WL' indicates word line, 'BIT' and 'BIT_B' represent bit line and bit line bar respectively. Monte Carlo simulations are run with -50% to +50% variation of the threshold voltage of CMOS transistors in SRAM cell and the leakage current of the cell is measured. The major source of intra-die V_t variation in SRAM array is RDF (Random Dopant Fluctuations). Since RDF induced V_t variation is completely random, the leakage of different cells can be considered as independent random variables. Figure 2 is the simulation result of the leakage current of SRAM cell with variation in V_t of NMOS transistors. Figure 2 shows that the leakage current is more for low V_t transistors with 0.08 V being the nominal V_t value of NMOS transistor.

Figure 3 is the simulation result of the leakage current of SRAM cell with variation in V_t of PMOS transistors. It shows that the leakage current is more for high V_t transistors with -0.2 V being the nominal V_t value of PMOS transistor. In both the cases, the leakage current of the SRAM cell is high for the transistors with V_t varied from its nominal value. This increase in leakage current through the transistor results in failure of the cell to retain the stored data causing the occurrence of hold failures.

In Fig. 4, N1 and N2 are storage transistors, P1 and P2 are load transistors and AXL and AXR are access transistors. When the cell is accessed through the row decoder, the node Z becomes high, hence N3 transistor is ON. This provides a ground path for source line (VSL) connected to source of N1 and N2 transistors. During the standby mode when the cell is not accessed, node Z becomes low, hence transistor P3 is ON. This provides a bias voltage (VSB) to the source line of N1 and N2 transistors, reducing the sub-threshold and gate leakage during the inactive periods. The impact of source bias on SRAM is analyzed by designing a row of 16 SRAM cells.

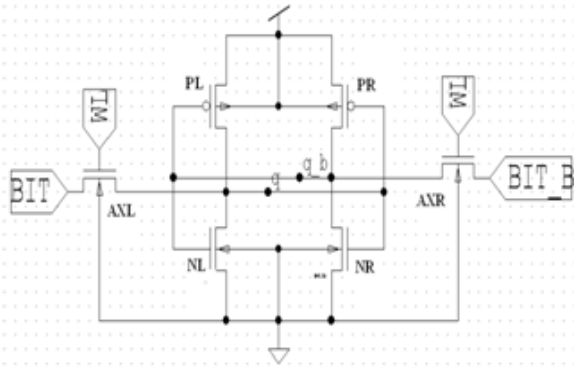

Fig. 1: Conventional 6T SRAM cell

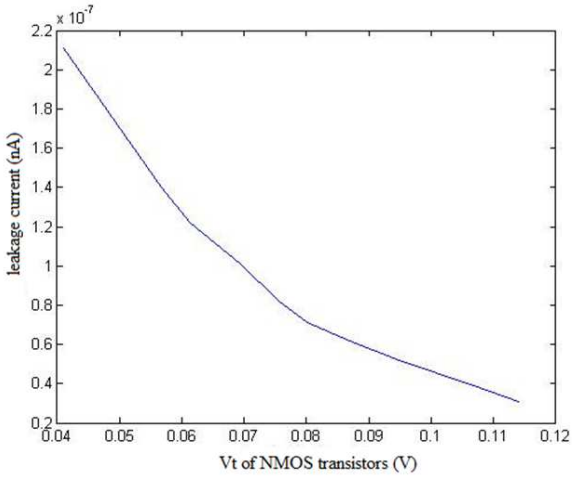

Fig: 2: Cell leakage with V_t variations in NMOS transistors

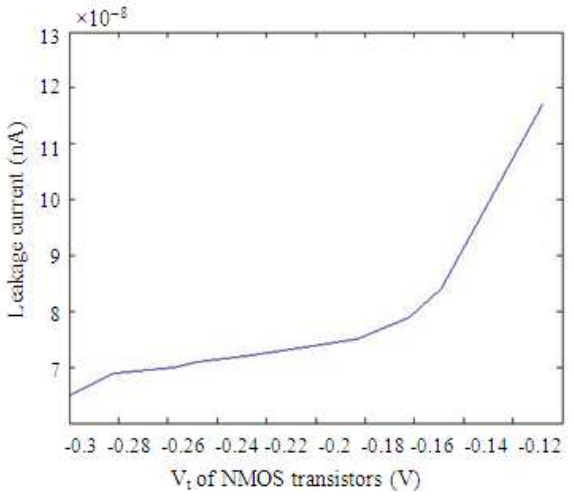

Fig. 3: Cell leakage with V_t variations in PMOS

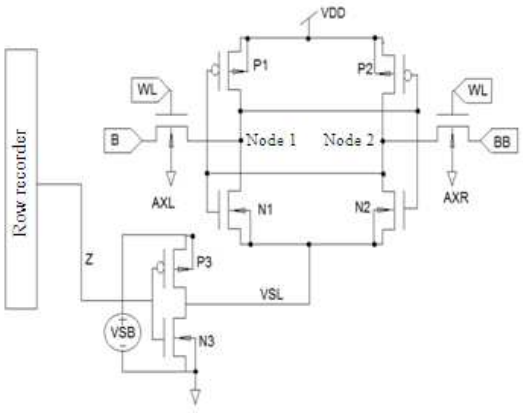

Fig. 4: Schematic of source biasing of SRAM cell

Impact of source bias on SRAM: The dominant leakage components of a SRAM cell are sub-threshold, gate and junction tunneling leakage. Process parameter variations, in particular V_t, causes significant variation in sub-threshold leakage. Source biasing is an efficient technique to reduce leakage. In standby mode, when the source line voltage of NMOS transistors NR and NL are biased (V_{SB}), the voltage of node storing '0' (q_b) increases from 0V to V_{SB}.

This results in a negative VGS (and negative VBS) operation of access transistor AXL, resulting in sub-threshold leakage reduction. Sub-threshold leakage of NMOS transistor NR is reduced due to a lower VDS and a negative VBS. Similarly, lower VDS to PMOS transistor PL reduce its sub-threshold leakage. Moreover, increasing the source bias reduces the rail-to-rail bias across the cell, reducing its gate leakage. Thus when source line is biased, substantial leakage savings can be obtained. Figure 4 shows the schematic of source biasing of single SRAM cell.

The simulation is performed by varying the source bias voltage from 0 to 350 mV during the standby mode and the simulated result is shown in Fig. 5. The results show that the leakage current is reduced, when source bias voltage is increased. When the source bias voltage is at '0' mV, leakage current is 280 nA and gets reduced as source bias voltage increases.

Impact of source bias on SRAM with Vt variations: Increasing the source bias voltage requires a higher VDDmin to hold the data. But the intra-die process variations results in fluctuations in VDDmin at which the data can be retained. Thus the principal reason for hold failure in SRAM cell is the intra-die variation in V_t.

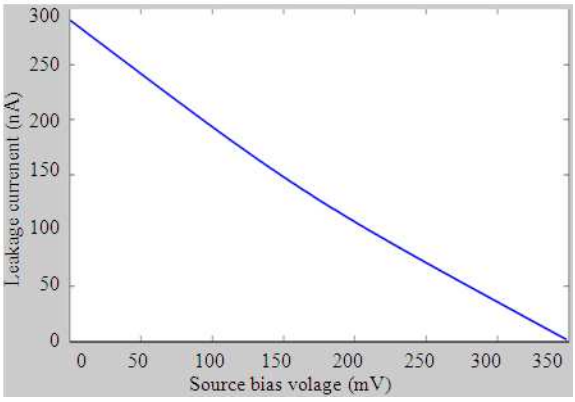

Fig. 5: Simulated output with leakage current in (nA) and voltage in (mV)

Due to process parameter variations when threshold voltage gets reduced (low Vt transistors) increases the leakage current through the transistor NL resulting in hold failures. Hence the Hold Failure Probability (PHF) in memory increases when Vt value gets varied from the nominal value. The PHF with respect to VDDmin for a source bias cell is given by:

$$P_{HF} = P(V_{DD\min} > (V_{DD} - V_{SB})) \quad (1)$$

Thus, when VSB is increased, the leakage current gets reduced. But it also reduces the supply voltage resulting in hold failure. Moreover, very high increase in VSB at the standby mode results in the loss of transistor characteristics. In hold mode, a column in an SRAM array is said to be faulty, if any of the cell in that column fails to hold the data. The faulty column is replaced by the redundant column but if the number of faulty column exceeds the number of redundant column then the array is said to be faulty. Hence, the maximum VSB is ultimately limited by the number of redundant columns.

Adaptive source biasing: In the stand-by mode, when the SRAM array is not accessed, source is biased. Fixed VSB cannot be applied to the SRAM array because it does not meet the targeted PHF and maximum leakage power reduction cannot be obtained. Hence, VSB is increased so that leakage power can be reduced as much as possible. However maximum VSB is limited by the Number of Redundant Columns (NRC) available to repair the faulty columns due to hold failures. So, the input for adaptive source biasing is the number of redundant columns. For 90 nm technology, without any parameter variation, VSB can be increased till 320 mV above which the transistor performance is lost. Let the number of redundant columns for a 8x16 SRAM array designed be 4.

Initially VSB starts from '0' mV and March algorithm is applied to identify the column failures in SRAM array. If number of column failures is greater than NRC then VSB is not further increased. If not, VSB is increased by ΔV (VSB = VSB + ΔV). For NRC to be 4, ΔV is 80 mV. The above conditions are again verified for VSB to be 80 mV and it is repeated until all the redundant columns are exhausted. Since VSB applied, starts from '0' mV, the number of March tests run, to determine the maximum VSB is more, increasing the test time. Hence, a DFT is proposed to reduce the test time using VSB predictor, which determines the maximum VSB with lesser number of March tests and is independent of the size of the SRAM array.

Proposed DFT with V_{sb} predictor: Choosing the initial VSB from '0' mV and reaching maximum VSB runs more number of March tests. Instead if a predicted VSB is used as the initial VSB then the number of March tests can be reduced. Moreover due to intra-die variation in Vth, the probability of cell hold failure or presence of weak cell is more at low and high Vth process corner. If in an SRAM array, the low and high Vth process corners are identified then weak cells can be easily detected. In the proposed DFT, a VSB predictor is designed and placed in each column of the SRAM array. It identifies the presence of weak cells in a particular column, which is independent of the size of the SRAM array.

If there is no weak cell then V_{SB} predicted is maximum (320 mV for 90nm technology). According to the presence of number of weak cells, V_{SB} is reduced. This predicted V_{SB} is then applied to the SRAM array and March test is run to identify the cells with hold failures. If it exceeds NRC, then predicted V_{SB} is the maximum V_{SB} that can be applied to the SRAM array in stand-by mode while maintaining the hold failure under control. In the proposed method maximum V_{SB} is reached starting from a predicted V_{SB} and not from '0' mV. Hence, the number of March tests is comparatively reduced saving the test time.

Proposed technique: In this study, a DFT technique capable of detecting weak cells using V_{SB} predictor is proposed. Figure 6 shows the block diagram of a V_{SB} predictor.

It consists of a row selector which is capable of accessing all the cells at a time. The Bit Line (BL) and Bit Line Bar (BLB) of all the cells in a column are connected together. BLB of all columns in the SRAM array are connected to the delay monitor placed at the end of each column.

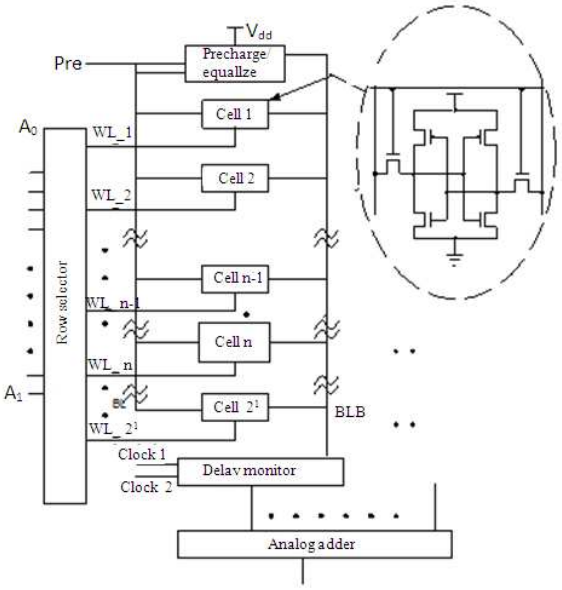

Fig. 6: Block diagram of V_{SB} predictor

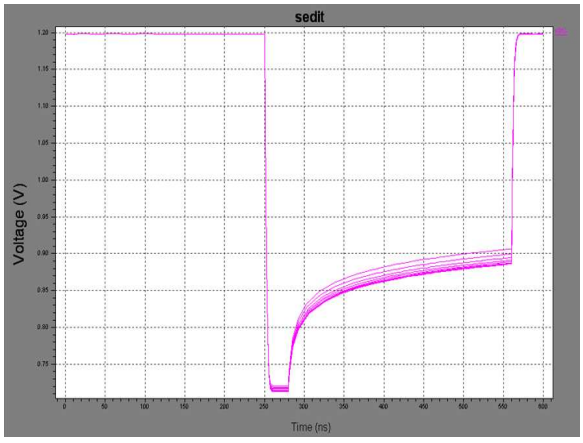

Fig. 7: Bit line bar capacitance charge path corresponding to different V_t

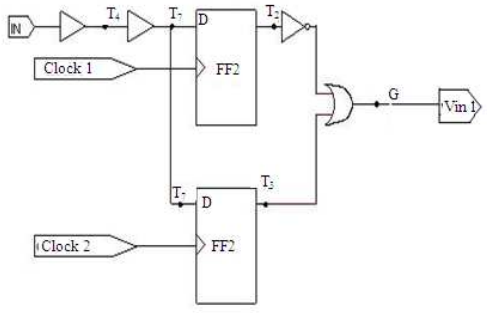

Fig. 8: Schematic of delay monitor circuit

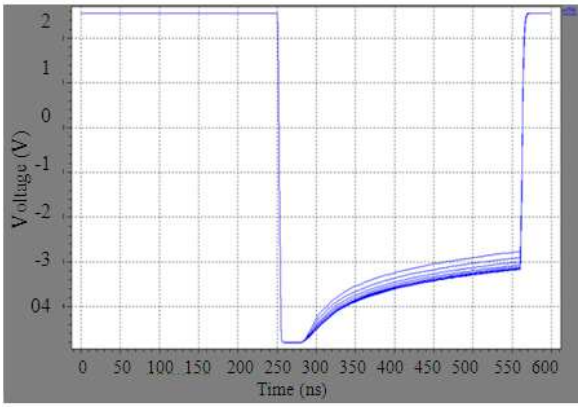

Fig. 9: Output of first amplifier at T_4

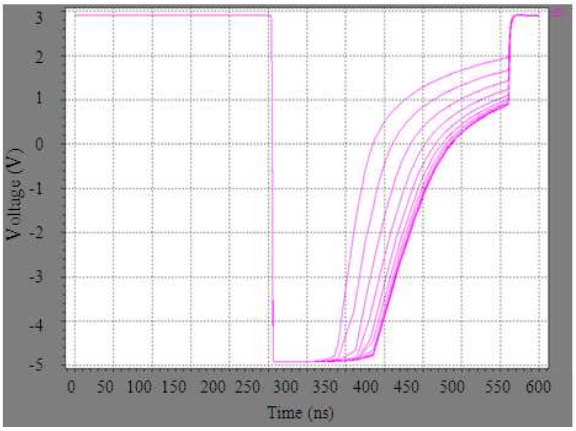

Fig: 10: Output of second amplifier at T_7

The output of all delay monitors are fed to the analog adder, which generates the corresponding V_{SB}. Initially all the cells are written zero at the same time. So BL = 0 and BLB = 1. Then both BL and BLB are pre charged by $V_{DD}/2$ and read operation is performed in parallel for all columns in the array. When the word lines are enabled at once, the capacitance of each bit line discharges according to the time constant created by the corresponding equivalent path. If there is any weak cell present in a particular column, BL of that column will take different discharge path.

To verify the proposed DFT technique an 8×16 SRAM array is designed. It has 8 columns with 16 cells in each and additional 20pF capacitor, to imitate more capacitive bit lines. A special row selector is used which is capable of selecting all the rows simultaneously, to initially write'0' in all cells in the array.

Figure 7 is the Monte Carlo simulation output for BLB.

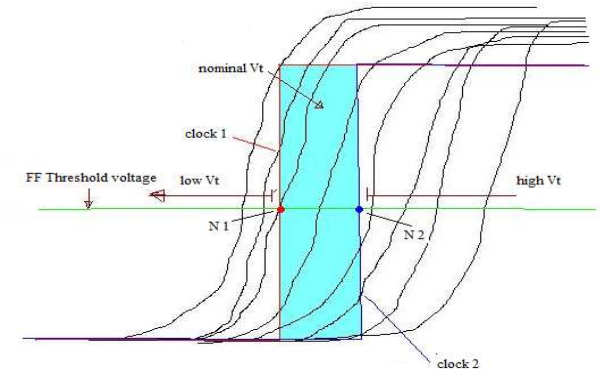

Fig. 11: Conceptual diagram of delay monitor circuit

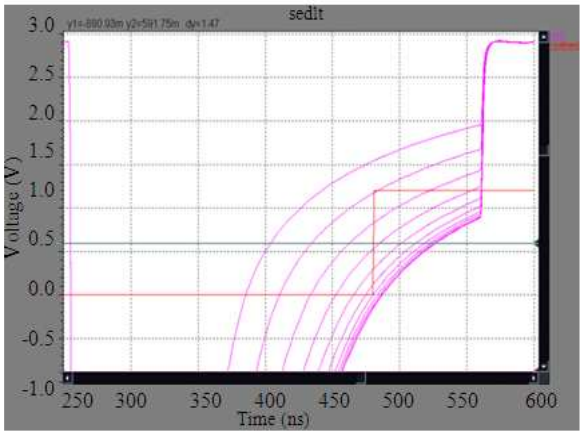

Fig. 12: Detection of charge path of nominal V_t

In each set of simulation, the threshold voltage of transistors are varied with -50% to +50% variation. From 0 to 250 ns write operation is performed, so BLB = 1(V_{DD} = 1.2V). Then BLB is pre charged by V_{DD}/2, so BLB = 0.6 V from 250 ns to 280 ns. After which read operation is performed, so BLB must reach V_{DD} but there exist a delay due to the capacitance effect of the BLB line. Due to intra-die V_t variation, if the transistors in a cell have low V_t then the charging of the capacitance will be quick but if the transistors in a cell have high V_t then the charging of the capacitance will be slow. Thus for charging the effective capacitance it will take different path corresponding to different V_t value. To identify the difference in the path of charging, a delay monitor circuit is connected to BLB.

Delay monitor: Figure 8 shows the schematic of a delay monitor circuit. It has two amplifiers with low slew rate.

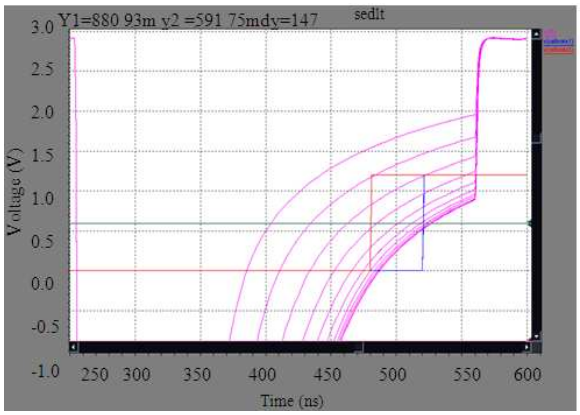

Fig. 13: Detection of charge path of nominal and high V_t

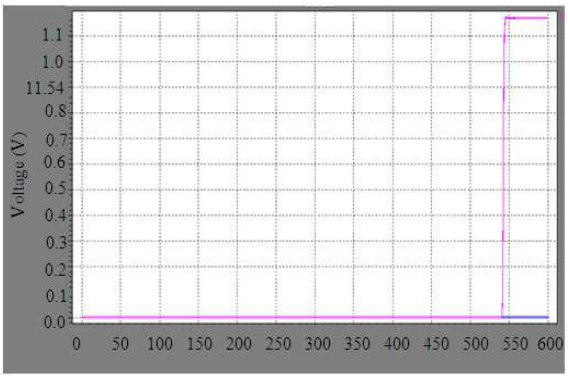

Fig. 14: Output of delay monitor circuit

The BLB line capacitance charging path is the input for the amplifiers. The delay between each charge paths will further increase and facilitates to separately analyze the different charge paths. Figure 9 is the output of the first amplifier at node T_4 and Figure 10 is the output of the second amplifier at node T_7 which shows the increase in delay between each charge paths. Two edge triggered D-flip-flops are used to sample the time dispersed charge path at different time instances with the help of two clocks, clock 1 and clock 2. Clock 2 is delayed with respect to clock 1 by 50 ns.

The basic principle of the delay monitor is that, low V_t transistors will have fast charging and high V_t transistors will have slow charging. This principle is used to determine the abnormal V_t cells (V_t above or below of acceptable limit). The operation of the delay monitor circuit is explained with the conceptual diagram of Fig. 11. The nominal V_t range is shown in the region of blue color.

The studying of each Flip Flop (FF) is such that the output will be one when the clock and the input voltage (BLB charge voltage) becomes above the threshold voltage of the FF. The charge path after N1 will make the FF 1 to be in ON state and the charge path after N2 will make the FF 2 to be in ON state. Hence FF 1 is ON for nominal V_t range and OFF during low and high V_t range. FF 2 is ON for high V_t range and OFF during low and nominal V_t range.

The output of the FF is connected to an inverter and OR gate, to encode the outputs of two flip flops such that the final output of the delay monitor circuit should be '1', when the charge path is not through the nominal V_t range. When the charge path is in the nominal range, FF 1 is in ON state and FF 2 is in OFF state. Hence the node G in Fig. 8 is low causing the potential of Vin1 to be '0'. When the charge path is below the nominal range (low V_t), FF 1 is in OFF state and when the charge path is above the nominal range (high V_t), FF 2 is in ON state. Both the conditions make the node G to be high causing the potential of Vin1 to be '1' indicating the presence of a weak cell. Vin1 is the output potential of the BLB capacitance charge path of a single column.

Figure 12 shows the charge paths with clock 1 signal (red line) capable of detecting nominal V_t. Figure 13 shows the charge paths with clock 1 signal (red line) and clock 2 signal (blue line) capable of detecting nominal $V_{t\ and}$ high V_t range.

Figure 14 shows the Monte Carlo simulation output of the delay monitor circuit, with variation in V_t. The pink line corresponds to the presence of low $V_{t\ and}$ high V_t cells in a column, causing the potential of the output of the delay monitor node to be at 1.2 V. Blue line corresponds to the presence of nominal V_t cells in a column, causing the potential to remain at 0 V. The output of the delay monitor circuit is fed to an analog adder.

Analog adder: The final module of the V_{SB} predictor is an analog adder which will suitably predict the maximum V_{SB} ($V_{SB(max)}$) to be applied. Figure 15 shows the schematic of an analog adder. It consists of an operational amplifier connected in negative feedback and a voltage source of 0.27 V is connected to the positive terminal of operational amplifier. Vin1 to Vin8 represent the delay monitor output of 8 columns of the SRAM array. The delay monitor output will be in logic '1' when any weak cells exist in the corresponding column. The outputs of the delay monitors are connected to the inputs of analog adder, such that if all the inputs are in logic '0' the output will be in 320mV ($V_{SB(max)}$), indicating absence of weak cells. If any of the input is in logic '1' state, output will be reduced.

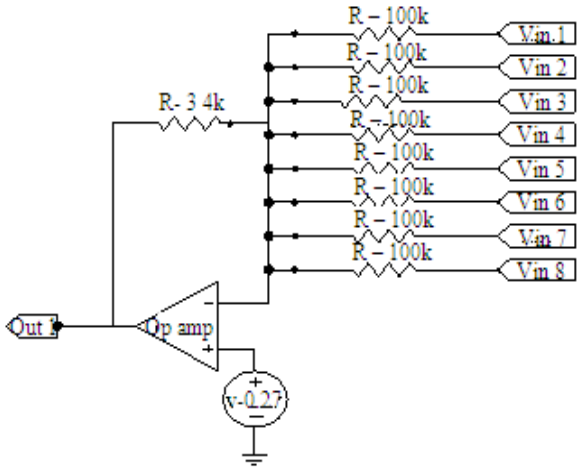

Fig. 15: Schematic of analog adder

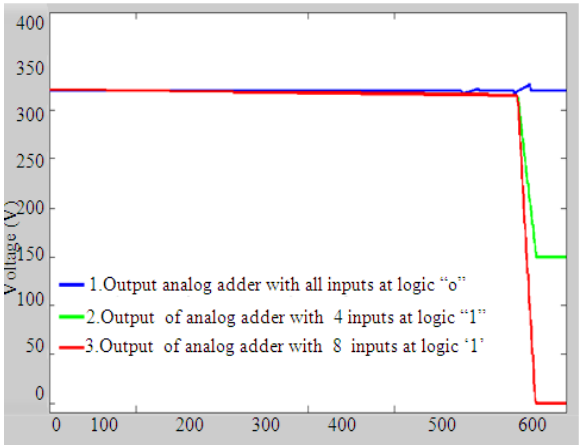

Fig. 16: Output of analog adder with different inputs

NDO represent the number of delay monitor outputs which is equal to the number of columns in the SRAM array. Hence with 8 delay monitor outputs and $V_{SB(max)}$ of 320 mV, ΔV_{SB} is 40 mV. Therefore, V_{SB} is reduced to 280 mV ($V_{SB\ (max)}$ - ΔV_{SB}).

Figure 16 shows the output of analog adder. It is reduced to 160 mV from $V_{SB(max)}$ of 320 mV, with four inputs at logic '1'. Likewise when the number of inputs with logic '1' increases, $V_{SB(max)}$ gets reduced. If all the inputs are in logic one, the output will be in '0' mV.

The amount of V_{SB} reduction (ΔV_{SB}) is given by:

$$\Delta V_{SB} = \frac{V_{SB(max)}}{NDO} \quad (2)$$

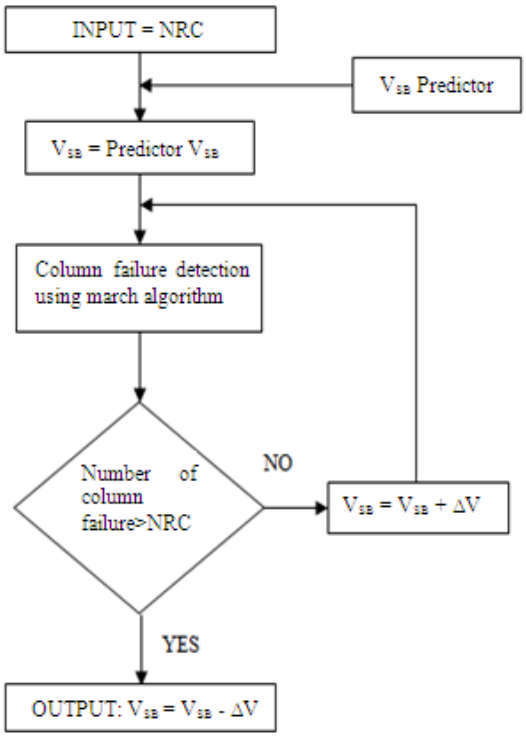

Fig. 17: Flow chart of proposed technique

Hence the entire system can be explained as,when there is no weak cell in any column of the SRAM array, the predicted V_{SB} will be in its maximum value. According to the increase in the number of columns with weak cell, the final output (i.e. predicted V_{SB}) will reduce.

The source bias voltage generated by the DFT is used as the initial source bias voltage instead of starting from '0' mV, to reduce the leakage current. This will reduce the number of March tests in predicting the V_{SB} because for each ΔV increment of V_{SB} one March test should run.

Time complexity analysis: Figure 17 shows the flow chart of the proposed technique. The input to the technique is the number of redundant columns. The source bias voltage predicted by the V_{SB} predictor is applied to the SRAM array. March algorithm is run to identify the column failures. If the number of column failures is more than NRC, V_{SB} is subtracted by ΔV (for NRC to be 4, ΔV is 30 mV) and it is fixed as the source bias voltage, to reduce the leakage current without any failures in SRAM array. If the number of column failures is less than NRC, V_{SB} is increased by ΔV and the procedure is repeated until all the redundant columns are exhausted.

In the proposed technique, the adaptive source bias starts from a predicted V_{SB} instead of from '0' mV. Let 'N' be the number of memory locations and 'T' be the memory access time in seconds. Then the total time taken for March test 't' is 'NT'. Hence the complexity of March test is in the order of O (N). For a 1 Mb SRAM array, with access cycle time assumed to be 10 ns. The test time required using March algorithm is 0.02 s.

To find the maximum V_{SB} if the algorithm starts from '0'mV, for every voltage applied, a March test has to run. Thus, if there are 'X' number of March tests run between V_{SB} = 0 mV and maximum $V_{SB,}$ the time required for finding the maximum V_{SB} is 'XNT'. If 'X' is assumed to be 5, then total test time is 0.1s. Therefore the complexity of the algorithm is O (XN), hence increases exponentially with 'X'.

But if the algorithm starts from a predicted initial $V_{SB,}$ then the number of March tests run to determine the maximum V_{SB} is reduced. It is because, the V_{SB} is predicted based on the presence of weak cells in the array, which are responsible for hold failures. Thus, with the predicted V_{SB} as initial V_{SB} applied to the SRAM array, maximum V_{SB} is determined with maximum of two March tests. Hence, the total test time is 0.04s, causing total test time reduction of about 60%. Moreover, the time taken to predict the initial $V_{SB,}$ is independent of the size of the SRAM array because all the cells in an array are accessed at the same time to perform the write operation followed by the read operation to determine the weak cells. If 'C' is the constant time taken for predicting the $V_{SB,}$ then the time required for finding out the maximum V_{SB} is 'CNT'. Hence the complexity of the March test remains in the order of O (N) and does not increases exponentially.

CONCLUSION

As the integration density of transistors increases, leakage power increases and degrades the parametric yield of SRAM. Hence, in this study a novel technique for low-leakage SRAM design has been proposed by utilizing the source biasing for reducing the leakage current and analyzed the impact of source bias on hold failure. The cells affected due to hold failures are replaced with available redundant columns. More number of March tests run, to identify the cells with hold failure, remains to be more time consuming. Hence in this study, a DFT is proposed to detect the presence of any weak cells in the columns of SRAM array and it will also predict an initial V_{SB}. The time taken to predict the initial source bias voltage is

independent of the size of the SRAM array and hence the time complexity of March tests does not increase exponentially. The timing analysis of the flowchart and simulated results indicates that the proposed system reduces the total test time by 60%.

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